Customer No.: 020991

CLAIMS

WHAT IS CLAIMED IS:

1. A method for transmitting encoded signals, the method comprising:

receiving one of a plurality of set of bits of a codeword from an encoder for transforming

Patent

an input message into the codeword;

non-sequentially mapping the one set of bits into a higher order constellation; and

outputting a symbol of the higher order constellation corresponding to the one set of bits

based on the mapping.

2. A method according to claim 1, further comprising:

writing N encoded bits to a block interleaver on a column by column basis; and

reading out the encoded bits on a row by row basis, wherein the block interleaver has N/3

rows and 3 columns when the higher order modulation is 8-PSK (Phase Shift Keying),

N/4 rows and 4 columns when the higher order modulation is 16-APSK (Amplitude

Phase Shift Keying), and N/5 rows and 5 columns when the higher order modulation

is 32-APSK.

3. A method according to claim 1, wherein the encoder in the receiving step generates

the codeword according to a Low Density Parity Check (LDPC) code.

4. A method according to claim 3, wherein the parity check matrix of the LDPC code

is structured by restricting a triangular portion of the parity check matrix to zero values.

5. A method according to claim 3, wherein the higher order constellation represents a

Quadrature Phase Shift Keying (QPSK) modulation scheme, the method further comprising:

determining an i^{th} QPSK symbol based on the set of $2i^{th}$ and $(2i+1)^{th}$ LDPC encoded bits,

wherein i=0,1,2..., N/2-1, and N is the coded LDPC block size.

52

Customer No.: 020991

Patent

6. A method according to claim 3, wherein the higher order constellation represents an 8-PSK modulation scheme, the method further comprising:

determining an i^{th} 8-PSK symbol based on the set of $(N/3+i)^{th}$, $(2N/3+i)^{th}$ and i^{th} LDPC encoded bits, wherein i=0,1,2,...,N/3-1, and N is the coded LDPC block size.

7. A method according to claim 3, wherein the higher order constellation represents a 16-APSK (Amplitude Phase Shift Keying) modulation scheme, the method further comprising:

determining an i^{th} 16-APSK symbol based on the set of $(N/2+2i)^{th}$, $2i^{th}$, $(N/2+2i+1)^{th}$ and $(2i+1)^{th}$ LDPC encoded bits, wherein i=0,1,2,...,N/3-1, and N is the coded LDPC block size.

8. A method according to claim 3, wherein the higher order constellation represents a 32-APSK (Amplitude Phase Shift Keying) modulation scheme, the method further comprising:

determining an i^{th} 32-APSK symbol based on the set of $(N/5+i)^{th}$, $(2N/5+i)^{th}$, $(4N/5+i)^{th}$, $(3N/5+i)^{th}$ and i^{th} LDPC encoded bits, wherein i=0,1,2,...,N/5-1, and N is the coded LDPC block size.

- 9. A computer-readable medium bearing instructions for transmitting encoded signals, said instruction, being arranged, upon execution, to cause one or more processors to perform the method of claim 1.
 - 10. A transmitter for generating encoded signals, the transmitter comprising: an encoder configured to transform an input message into a codeword represented by a plurality of set of bits; and

logic configured to map non-sequentially one set of bits into a higher order constellation, wherein a symbol of the higher order constellation corresponding to the one set of bits is output based on the mapping.

Customer No.: 020991

Patent

11. A transmitter according to claim 10, wherein the *N* encoded bits are written to a block interleaver column by column and read out row by row, and the block interleaver has *N*/3 rows and 3 columns when the higher order modulation is 8-PSK (Phase Shift Keying), *N*/4 rows and 4 columns when the higher order modulation is 16-APSK (Amplitude Phase Shift Keying), and *N*/5 rows and 5 columns when the higher order modulation is 32-APSK.

- 12. A transmitter according to claim 11, wherein the encoder generates the codeword according to a Low Density Parity Check (LDPC) code.
- 13. A transmitter according to claim 12, wherein the parity check matrix of the LDPC code is structured by restricting a triangular portion of the parity check matrix to zero values.
- 14. A transmitter according to claim 12, wherein the higher order constellation represents a Quadrature Phase Shift Keying (QPSK) modulation scheme, and the logic is further configured to determine an i^{th} QPSK symbol based on the set of $2i^{th}$ and $(2i+1)^{th}$ LDPC encoded bits, wherein i=0,1,2...,N/2-1, and N is the coded LDPC block size.
- 15. A transmitter according to claim 12, wherein the higher order constellation represents an 8-PSK modulation scheme, and the logic is further configured to determine an i^{th} 8-PSK symbol based on the set of $(N/3+i)^{th}$, $(2N/3+i)^{th}$ and i^{th} LDPC encoded bits, wherein i=0,1,2,...,N/3-1, and N is the coded LDPC block size.
- 16. A transmitter according to claim 12, wherein the higher order constellation represents a 16-APSK (Amplitude Phase Shift Keying) modulation scheme, and the logic is further configured to determine an i^{th} 16-APSK symbol based on the set of bits $(N/2+2i)^{th}$, $2i^{th}$, $(N/2+2i+1)^{th}$ and $(2i+1)^{th}$ LDPC encoded bits, wherein i=0,1,2,...,N/3-1, and N is the coded LDPC block size.
- 17. A transmitter according to claim 12, wherein the higher order constellation represents a 32-APSK (Amplitude Phase Shift Keying) modulation scheme, and the logic is further configured to determine an i^{th} 32-APSK symbol based on the set of bits $(N/5+i)^{th}$,

Customer No.: 020991

Patent

 $(2N/5+i)^{th}$, $(4N/5+i)^{th}$, $(3N/5+i)^{th}$ and i^{th} LDPC encoded bits, wherein i=0,1,2,...,N/5-1, and N is the coded LDPC block size.

18. A method for processing encoded signals, the method comprising:

demodulating a received encoded signal representing a codeword, wherein the encoded signal being modulated according to a non-sequential mapping of a plurality of bits corresponding to the codeword; and decoding the codeword associated with the encoded signal.

- 19. A method according to claim 18, wherein the *N* encoded bits are written to a block interleaver column by column and read out row by row, and the block interleaver has *N*/3 rows and 3 columns when the higher order modulation is 8-PSK (Phase Shift Keying), *N*/4 rows and 4 columns when the higher order modulation is 16-APSK (Amplitude Phase Shift Keying), and *N*/5 rows and 5 columns when the higher order modulation is 32-APSK.
- 20. A method according to claim 19, wherein the decoding step is according to a Low Density Parity Check (LDPC) code.
- 21. A method according to claim 20, wherein the parity check matrix of the LDPC code is structured by restricting a triangular portion of the parity check matrix to zero values.
- 22. A method according to claim 20, wherein the higher order constellation represents a Quadrature Phase Shift Keying (QPSK) modulation scheme, and an i^{th} QPSK symbol is determined based on the set of $2i^{th}$ and $(2i+1)^{th}$ LDPC encoded bits, wherein i=0,1,2...,N/2-1, and N is the coded LDPC block size.
- 23. A method according to claim 20, wherein the higher order constellation represents an 8-PSK modulation scheme, and an i^{th} 8-PSK symbol is determined based on the set of $(N/3+i)^{th}$, $(2N/3+i)^{th}$ and i^{th} LDPC encoded bits, wherein i=0,1,2,...,N/3-1, and N is the coded LDPC block size.

Customer No.: 020991

Patent

24. A method according to claim 20, wherein the higher order constellation represents a 16-APSK (Amplitude Phase Shift Keying) modulation scheme, and an i^{th} 16-APSK symbol is determined based on the set of bits $(N/2+2i)^{th}$, $2i^{th}$, $(N/2+2i+1)^{th}$ and $(2i+1)^{th}$ LDPC encoded bits, wherein i=0,1,2,...,N/3-1, and N is the coded LDPC block size.

- 25. A method according to claim 20, wherein the higher order constellation represents a 32-APSK (Amplitude Phase Shift Keying) modulation scheme, and an i^{th} 32-APSK symbol is determined based on the set of bits $(N/5+i)^{th}$, $(2N/5+i)^{th}$, $(4N/5+i)^{th}$, $(3N/5+i)^{th}$ and i^{th} LDPC encoded bits, wherein i=0,1,2,...,N/5-1, and N is the coded LDPC block size.
- 26. A computer-readable medium bearing instructions processing encoded signals, said instruction, being arranged, upon execution, to cause one or more processors to perform the method of claim 18.